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Reduced Power Flip Flop Design for Clock Distribution Networks

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ABSTRACT— ***In this paper a technique is proposed to reduce the power consumption in clock distribution networks. Power has become a major issue in most VLSI designs. Power distribution in VLSI differs from product to product. However it is interesting to note that clock system and logic part itself consume most of total chip power. In practise a large portion of clock distribution network (CDN)s and flip flops. In this paper a reduced power flip flop design is used in CDNs. The simulations are done using Microwind and DSCH analysis software tools.***

***Keywords*— Flip-flop, full swing low swing, power, resonant clock**

I. INTRODUCTION

In all kinds of digital designs flip flops are the basic storage elements. In particular digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that in many VLSI systems the power consumption of clock system comprising of CDN and storage elements consumes large amount of total power

In complex VLSI, significant amount of power is consumed by the clocking networks. The global nature of clock distribution interconnects and increased parasitic with scaling further results in the increased power consumption. The CDN of microprocessor is typically divided into global and local clock distributions. The global clock distribution comprises a clock source and the wires and buffers needed to drive the clock source to the logic gates. The local clock distribution network comprises of wires that connect to the clock loads-latches and gates- in the microprocessors functional units.

Reducing the supply voltage is an attractive approach to reduce power but has a quadratic effect on power consumption. However, we need to decrease the transistor threshold voltage for scaling down the supply voltage. This leads to substantial increase in leakage power. In addition, decreasing the supply voltage would increase system susceptibility to variations. As a result, there is an increasing demand for power reduction schemes that do not require a reduction in the supply voltage.

An emerging technique to reduce the power of the CDN is resonant clocking where low energy dissipation is achieved by recycling the energy stored on the clock capacitance. The three most common resonant clocking techniques include standing-wave resonant clocking, rotary travelling-wave resonant clocking and LC resonant clocking. Of these LC resonant clocking is the most convenient since it requires minimum change from conventional square wave designs.

In this paper, we introduce a Reduced Power Flip Flop(RPFF) for use in low swing LC resonant CDNs.

The remainder of this paper is organized as follows. A description of the existing full swing system is presented in Section II. Section III gives a description of the proposed RP-FF and a characterisation of delay associated with low swing clocking. Simulation and measurement results obtained are conferred in section IV. The conclusion of this paper is provided in Section V.

II. EXISTING SYSTEM

The Differential Conditional Capturing Flip Flop (DCCFF) is shown in Fig. 1. Flip flop power is reduced at low data switching activities by eradicating unwanted transitions by a technique called conditional capturing. The DCCFF operates in a precharge and evaluate fashion. *SET* and *RESET* nodes are charged using pull-up PMOS transistors MP_1 and MP_2. By ensuring a constant path to *VDD* the effect of charge sharing is minimized. This is done by properly sizing the PMOS transistors. A short evaluation interval occurs after the rising edge of the clock when both the clock and inverted clock signals applied to transistors MN1/MN2 are above the threshold voltage level

of the NMOS transistor. This type of flip flop design uses full swing clocking. By modifying this circuit and using

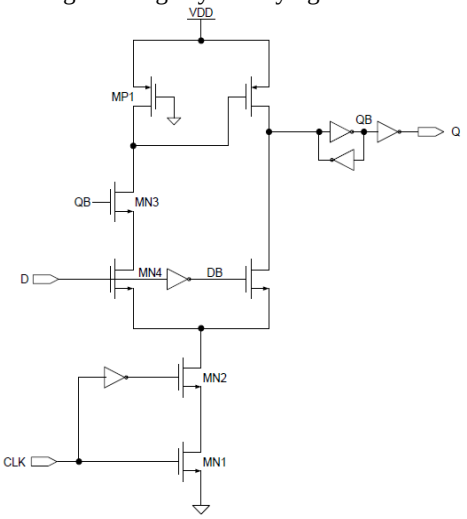

Fig. 1 DCCFF(full swing system)

low-swing clocking system we shall reduce the power consumption. The next section gives a detailed view of low-swing system.

III. LOW SWING FLIP FLOP

Fig. 2 shows the proposed Reduced Power Flip Flop (RPFF) design for clock distribution networks. Flip flop power is reduced at low data switching activities by eradicating unwanted transitions by a technique called conditional capturing [8]. From Fig. 2, reduced swing inverters similar to the one presented in [7] is used. The load pMOS transistor in the reduced swing inverters is always in saturation since. When the low swing clock signal reaches its peak voltage, the load pMOS transistors in saturation lowers the voltage at the source of second pMOS in each inverter thereby turning it off. The peak voltage for reduced swing clock was chosen to be equal to 0.65 V since 1 V and 0.34 V is the approximate threshold voltage of the pMOS transistor.

A. *Delay in Reduced Swing system*

In Fig 3, $V_{\square\square\square\square\square\square}$ is the voltage level at which transistor MN1 with the clock signal applied to its gate pulls down node SET/RESET to the low voltage level required to

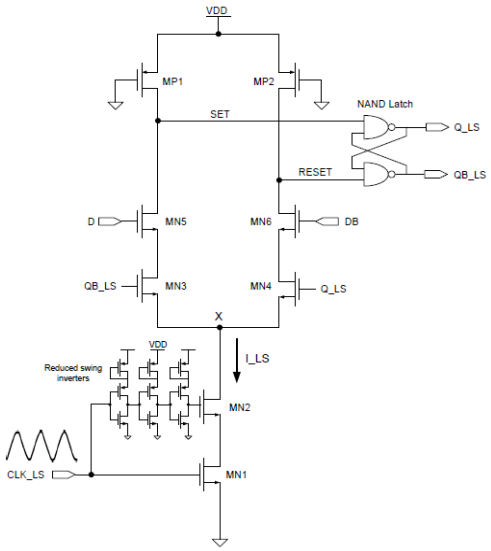

Fig. 2 Reduced Power Flip Flop (RPFF)

An analysis is conducted to estimate the delay in reaching $V_{\square\square\square\square\square\square}$ for the low swing clocking. Assume the low and full swing clock signals be represented by the following equations:

$$V(\square) = \frac{1}{2} V_{DD} \sin\left(2\pi \square - \frac{\pi}{2}\right) + \frac{1}{2} V_{DD} \quad (1)$$

$$V(\square) = \frac{0.65}{2} V_{DD} \sin\left(2\pi \square - \frac{\pi}{2}\right) + \frac{0.65}{2} V_{DD} \quad (2)$$

where $\square$ is the clock frequency, V_{DD} and $0.65V_{DD}$ are respectively the peak voltage for the full- and low-swing clock signals

Depending on the input state, either node *SET* or *RESET* is pulled down to trigger the NAND latch when the clock signal reaches V_{Pull_down}. and referring to Fig. 3:

$$V(\square) = \frac{1}{2} V_{DD} \sin\left(2\pi \square_1 - \frac{\pi}{2}\right) + \frac{1}{2} V_{DD} \quad (3)$$

from which:

$$T_1 = \frac{1}{2\pi\square} \sin^{-1}\left(\frac{V_{\square\square\square\square\square\square}}{V_{DD}/2} - 1\right) + \frac{\pi}{2} \quad (4)$$

Similarly for the low-swing clock signal:

$$T_2 = \frac{1}{2\pi\square} \sin^{-1}\left(\frac{2V_{\square\square\square\square\square\square}}{0.655\, V_{DD}} - 1\right) + \frac{\pi}{2}$$

=

trigger the NAND latch. The low-swing flip-flop experiences longer data to output delay (TDQ) compared to the full-swing flip-flop for the same setup time (TDCLK) by virtue of the time difference between low and full swing

clock to reach $V_{\blacksquare\blacksquare\blacksquare\blacksquare}$

The *TDQ* delay between the low- and full-swing flip-flops is given by:

$$T_{D\blacksquare\blacksquare\blacksquare\blacksquare y} = T_2 - T_1$$

$$= \frac{1}{2\pi\blacksquare}\sin^{-1}\frac{2V_{\blacksquare\blacksquare\blacksquare\blacksquare\blacksquare}}{0.655\,V_{DD}} - 1 + \pi - \frac{1}{2\pi\blacksquare}\sin^{-1}\frac{V_{\blacksquare\blacksquare\blacksquare\blacksquare}}{V_{DD}}$$

$$1+\pi 2 \qquad 2 \qquad 2\pi\blacksquare \qquad (6)$$

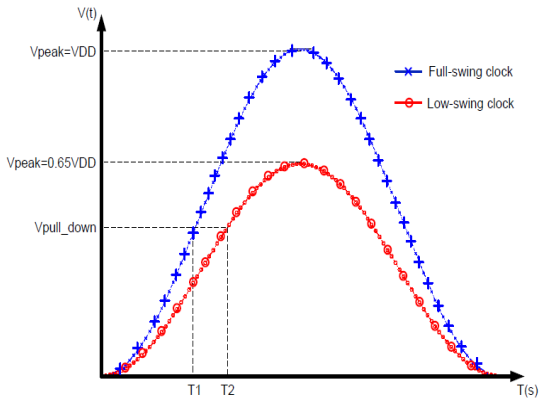

Fig. 3 Delay between the low- and full-swing resonant clock signals to reach $V_{\blacksquare\blacksquare\blacksquare\blacksquare}$

Equation (4.6) gives the delay between the full- and low-swing flip-flops. It illustrates that this delay is inversely proportional to clock frequency, i.e., at higher frequencies, the delay decreases.

IV. SIMULATION RESULTS

A. Full Swing System

Full swing differential conditional capturing flip flop have been simulated using microwind and DSCH tools. The circuit is first drawn on DSCH. Its simulated to get the timing diagram. A very log file is created and is compiled in Microwind to get the final graph and power consumption.

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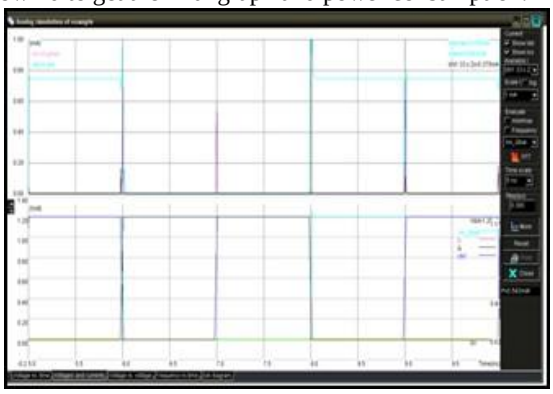

Fig. 4 Power characteristics of full swing system

Full swing system for reducing the power consumption has been evaluated by simulated using microwind and DSCH tools.Power consumption ≈ 0.543mW Area consumption ≈ 26× 480$\mu\blacksquare^2$

B. Low-Swing System

RPFF for reducing the power consumption has been evaluated by simulating using microwind and DSCH tools. The circuit is first drawn on DSCH. It's simulated to get the timing diagram. A very log file is created and is compiled in Microwind to get the final graph and power consumption. The measured results are as follows:

Power consumption ≈ 26× 650$\mu\blacksquare^2$

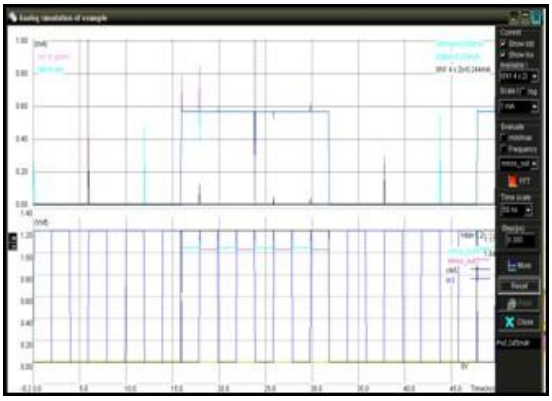

Fig. 5 Power characteristics of low swing system

TABLE 1 AREA AND POWER COMPARISON BETWEEN FULL-SWING AND LOW-SWING SYSTEM

Type	Power consumption	Area consumption
Full Swing design	0.543mW	26× 480μ
Low swing design	0.245mW	26× 650μ

V. CONCLUSION

The reduced power flip flop proposed in this paper uses low swing clocking and conditional capturing to reduce the power consumption. In addition double edge clocking can be incorporated into the flip flop to build clocking systems. We conclude this paper by emphasizing the fact that low swing flip flop designs offer better power reduction than low swing systems for clock distribution systems. By proposing this reduced power flip flop design for CDNs, power consumption of VLSI systems can be significantly reduced.

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