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# Forward Error Correction Scheme for High Speed Wireless Communication

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***ABSTRACT****-This paper focus on basic error correction detection i.e. especially forward error correction (FEC) scheme. Error Correction scheme increase the capacity by adding redundant information for the data transmission. The FEC code is used to secure data and information sent over the channel for storage as well as recover even in the presence of noise (errors). There are various error schemes like RS code, turbo code, convolution encoder, FEC, We introduce convolution encoder for encoding side and Viterbi Decoder for decoding side .Convolution encoding is a forward error correction technique which is used for correction of errors at the receiver side. Viterbi decoding is the technique for decoding the Convolution codes which is based on maximum likely hood decoding .this paper contributed works on basic techniques for error correction and detection.*

**Keywords:FEC. Convolution encoder. Viterbi decoder. BER.**

## 1, INTRODUCTION

Various fields like wireless communication, computer science, error detection and correction has great practical importance for maintaining data (information) integrity across noisy channels and less reliable storage media. A channel code is a term, which is broadly used, referring to the forward error correction (FEC) code and bit interleaving in communication and storage where the communication media or storage media is viewed as a channel.

Wireless medium is quite different as compared to wire but provides several advantages, like; better productivity, mobility, low cost, scalability and easy installation facility. Along with these there are some restrictions and disadvantages of various transmission channels in wireless medium between transmitter and receiver where transmitted signals reach at receiver with different time delay and power due to the diffraction, reflection, and scattering effects [3].

Besides the BER (Bit Error Rate) value of the wireless medium is relatively high. These disadvantages sometimes introduce destructive effects on the wireless communication [5]. Hence error control is necessary in these applications. During digital data transmission and storage operations, performance criterion is commonly determined by BER which is simply: Number of error bits / Number of total bits. Noise in transmission medium disturbs the signal and causes data corruptions [12].

In telecommunication, information theory, and coding theory, forward error correction (FEC) or channel coding [1] is a technique used for controlling errors in data transmission over unreliable or noisy communication channels. The central idea is the sender encodes their message in a redundant way by using an error-correcting code (ECC). The American mathematician Richard Hamming pioneered this field in the 1940s and invented the first error-correcting code in 1950: the Hamming (7,4) code.

The redundancy allows the receiver to detect a limited number of errors that may occur anywhere in the message, and often to correct these errors without retransmission. FEC gives the receiver the ability to correct errors without needing a reverse channel to request retransmission of data, but at the cost of a fixed, higher forward channel bandwidth. FEC is therefore applied in situations where retransmissions are costly or impossible, such as one-way communication links and when transmitting to multiple receivers in multicast. FEC information is usually added to mass storage devices to enable recovery of corrupted data, and is widely used in modems.

FEC processing in a receiver may be applied to a digital bit stream or in the demodulation of a digitally modulated carrier. For the latter, FEC is an integral part of the initial analog-to-digital conversion in the receiver. The Viterbi decoder implements a soft-decision algorithm to demodulate digital data from an analog signal corrupted by noise. Many FEC coders can also generate a bit-error rate (BER) signal which can be used as feedback to fine-tune the analog receiving electronics. The maximum fractions of errors or of missing bits that can be corrected is determined by the design of the FEC code, so different forward error correcting codes are suitable for different conditions.

## 2. METHODS: DIFFERENT SCHEME FOR FORWARD ERROR CORRECTION

There are several ways of classifying the forward error correction codes as per different characteristics [1]. Linear vs. Nonlinear- Linear codes are those in which the sum of any two valid code words is also a valid code word. In case of nonlinear code the above statement is not always true. The below fig.1 shows classification of FEC code.

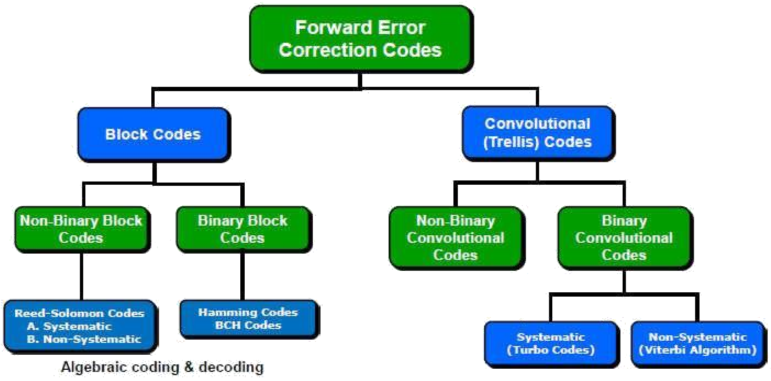
Forward Error Correction Codes
Block Codes
Convolutional (Trellis) Codes
Non-Binary Block Codes
Binary Block Codes
Non-Binary Convolutional Codes
Binary Convolutional Codes
Reed-Solomon Codes A. Systematic B. Non-Systematic
Hamming Codes BCH Codes
Systematic (Turbo Codes)
Non-Systematic (Viterbi Algorithm)
Algebraic coding & decoding

**Fig**.1 Classification of FEC codes

1. Cyclic vs. Non-Cyclic - Cyclic code word are those in which shifting of any valid code word is also a valid code word. In case of non-circular code word the above statement is not always true.

2. Systematic vs. Nonsystematic- Systematic codes are those in which the actual information appears unaltered in the encoded data and redundant bits are added for detection and correction of error. In non-systematic code the actual message does not appear in its original form in the code rather there exists one mapping method from the data word to code word and vice versa.

3. Block vs. convolution -The block codes are those in which one block of message is transformed into on block of code. In this case no memory is required. In case of convolution code a sequence of message is converted into a sequence of code. Hence encoder requires memory as present code is combination of present and past message.

4. Binary vs. Non binary -Binary codes are those in which error detection and correction is done on binary information i.e. on bits. Hence after the error is located, correction means only flipping the bit found in error. In Non-binary code error detection and corrections are done on symbols, symbols may be binary though. Hence both the error location and magnitude is required to correct the symbol in error.

➢ **Others error correct codes**

i. CRC coding
ii. RS coding
iii. BCH coding
iv. Block code
v. Turbo code

## 2.1 EXPERIMENTS: CONVOLUTION CODING

Convolution coding is a bit-level encoding technique. Convolution codes are used in applications that require good performance with low implementation cost. Using convolution codes a continuous sequence of information bits is mapped into a continuous sequence of encoder output bits. The encoded bits depend not only on current input bits but also on past input bits. This mapping is highly systematic so that decoding is possible. As compared with the block codes, convolution codes have a larger coding gain.[6]

## 2.2 CONVOLUTION ENCODER

The convolution encoder maps a continuous information bit stream into a continuous bit stream of encoder output. The convolution encoder is a finite state machine, which is a machine having memory of past inputs and also having a finite number of different states. The number of output bits depends on the number of modulo 2-adders used with the shift registers.[5]. Figure 2 shows the basic structure of convolution Encoder.

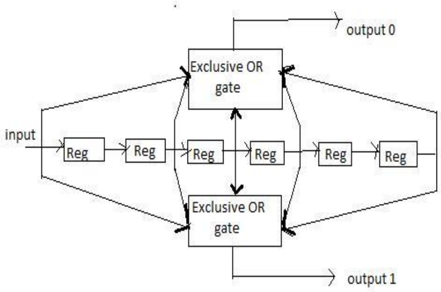

**Fig**. 2: A convolution Encoder

### 2.3 Convolution Encoder parameters

Convolution codes are commonly specified by the three parameters ($n$,$k$,$m$), where

$n$ = number of output bits

$k$ = number of input bits and,

$m$ = number of shift registers.[5]

Commonly $k$ and $n$ parameters range from 1to8,$m$from 2to10,and the code rate from 1/8 to 7/8 except for deep space applications where code rates as low as 1/100 or even longer can be employed.[4] The convolution codes discussed here will be referred as ($n$, $k$, $m$) codes. .[1]

Passing the information se quence to be transmitted through a linear finite shift register generates a Convolution c ode. The shift register consists of k bit stages and n linear algebraic function generat ors. The contents of shift register are multiplied by respective term in generator matrix and are then XORed together to generate re spective generator Polynomials.[8]

### 2.4 Generator Polynom ial

Generator Polynomial is defined by-

$$g^{(i)}(D)=g_0^{(i)}g_1^{(i)}(D)+g_2^{(i)}(D^2)+\ldots\ldots..+g_m^{(i)}(D^m) \quad \text{eq (1)}$$

Where ,D = unit delay variable

m = number of stages of shift registers.

The encoder connections are characterized by the term generator p olynomial (g). For producing the output bits the selection of which bits (in the memory registers) are to be added (using modulo-q adders) is called the generator polynomial for that output bit. Various choices are availab le for polynomials for any m order code. I t is again a task to find good polynomials whic h are normally found by trial and error meth od using computer simulations.[1][5]

***Example: (2, 1, 3) Convol ution encoder***

For understanding the working of a convolution encoder and the forwa rd error correction technique, we have taken t he following assumptions.

(a) We are using a (2, 1, 3) convolution encoder.

(b) A 3-bit input sequence [1 0 1] is specified bits.

(c) 2 generator polynomia ls [1 1 1] and [1 0 1] are used.

Figure 3 is a (2, 1, 3) convolution encoder. This encoder is going to be used to encode the 3-bit input sequence [1 0 1 ] with the two generator polynomials specified by the bits [1 1 1] and [1 0 1]. u1represents the input bit, and v 1and v2represent theoutputbits1and2respectively.*u0 andu-1* represent the initial state of the memory registers which are initially set to zero.[1][4][2]

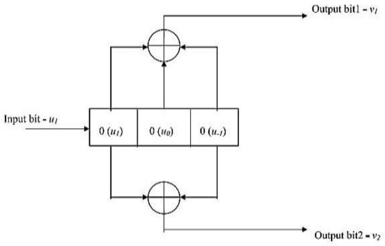

Fig.3: A (2,1,3) convolution encoder

## 2.5 State representation of convolution encoder

The convolution encoder can use a look-up table, otherwise callled the state transition table to do the encoding. The state transition table co nsists of four items:[6][7]

a) The input bit.
b) The state of the enco der, which is one of the 4 possible states (00011011) for the (2, 1, 3) convoluti on
encoder.
c) The output bits, whic h for the (2, 1, 3) convolution encoder ar e: 00011011, since only two bits are output.
d) The output state whic  is the input state for the next bit.

### 2.6 State Diagram Repr esentation

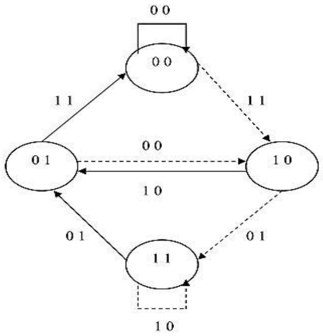

Fig.4: State diagram for the (2, 1, 3) convolution encoder [1]

### 3 (a) VITERBI DECODE R

Viterbi decoders work on Viterbi algorithm to decode the encoded data. The Viterbi decoding algorithm was discovered and analyzed by Viterbi in 1967. The Viterbi algorithm essentially performs maximum likelihood decoding; however, it reduces the computational load by taking advantage of the special structure in the code trellis [8] .

Viterbi Decoders (VDs) are today widely used as forward error correction (FEC) devices in many digital communicatio ns and multimedia products, including mobile (cellular) phones, video and audio broadcasting receivers, and modems. VDs are impl ementations of the Viterbi Algorithm (VA) used for decoding convolution or trellis codes.

The continuing success of convolution and trellis codes for FEC applications in almost all modern digital communication and multimedia products is based on three main factors:[18]

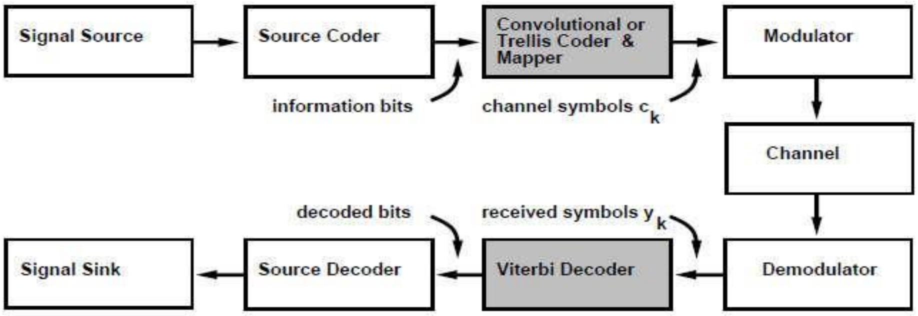

Fig .5 Basic Viterbi Decoders block diagram in Digital Communication systems [18].

### 2.7 Viterbi Decoding Technique

The Viterbi decoder examines an entire received sequence of a given length .The decoder compute same trick for each path and make decision based on this metric .All paths are followed until two paths converge on one node. When two paths enter the same state, the one having the best metric is chosen; this path is called the surviving path. The early rejection of the unlikely paths reduces the decoding Complexity [4][7][8]

### 2.8 Block Diagram of Viterbi Decoder

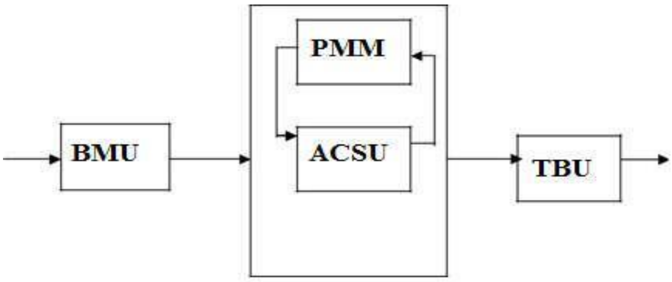

**Fig**.6: Block diagram of Viterbi Decoder

1) Branch metric unit (BMU): From the encoder output through the channel the BMU receives input data and computes a metric for each state and each input bit. BMU compares the received data bits are compared with the expected or idel outputs and counts the number of differing bits [8].

2) Path Metric Unit: The path metric unit includes the Add compare and select unit. The partial path metrics are compared by the comparator and branch metric is selected by the selector. That means the selector selects the smaller value.[9]

3) Add-Compare Select unit (ACSU): The Add-Compare Select Unit (ACSU) adds the Branch Metrics (BM) to the partial Path Metrics (PM) to obtain new path metric. When two paths enter the same state, it compares the new PMs and the one having minimum metric is chosen , this path is called survivor path. The selection for survivor path is done for all states. It then stores the selected PMs in the Path Metric Memory (PMM). The PM of the survivor path of each state is updated and stored back into the PMM [8].

## 3. RESULT

The below result shows the reference result (fig.7) for FEC uncoded convolution code with AWGN channel [15]. The error performance for ½ rates is best as compare to uncoded and other rates. Figure 8 depict the reference result for Viterbi decoder.

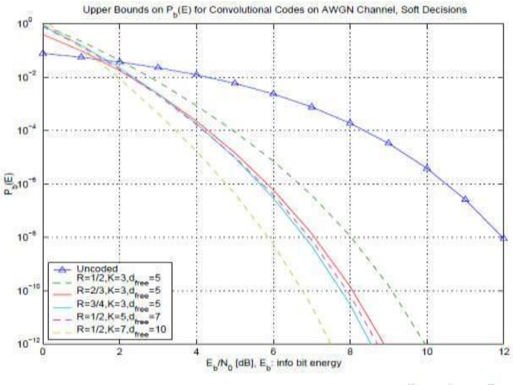

Fig.7 reference result for uncoded and convolution code AWGN channel [15]

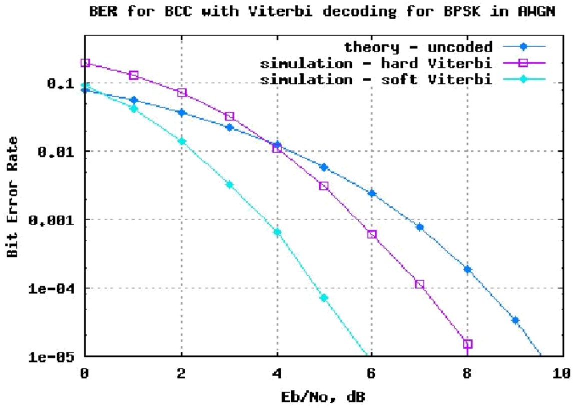

Fig.8 reference result for BER plot for BPSK with AWGN in soft deci sion Viterbi decoding[16]

## 4. CONCLUSION

The design of a convolutio n encoder with a Viterbi decoder that can e ncode a bit stream of digital information and outputs a code word that has a capability to be transmitted to the destination and then d ecoded .The encoder was designed with a re spective rate .The Viterbi decoder design had been driven in

such a way that it would calculate the decoding path with the mini mum metric to be passed to the decoder output port. Convolution encoder and Viterbi decoder will be design using MATLAB an d results will be obtain in terms of BER vs. SNR..it is to be found that, the for FEC basically the convolution encoder and Viterbi decoder will provide good acceptable performance/result.

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