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PIPELINED ADC WITH A TRANSCONDUCTANCE OPERATIONAL AMPLIFIER IN FINFET TECHNOLOGY

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Abstract—*The comparator is designed in pipelined ADC. FINFET is the technology which performs the dual gate MOSFET. This thesis focuses on the high-speed design of pipelined ADC. In the meanwhile, we try to minimize the power dissipation as well. In this thesis, A semi-digital Gm-based amplifier is proposed for a low-power pipelined analog-to-digital converter (ADC)in HSPICE .And also we compare the power performance both in FINFET and CMOS. The amplifier performs a class-AB operation. CMOS designed in 130nm and FINFET is implemented in 16nm.*

Keywords—***Analog-to-digital converter (ADC, Gm-based amplifier, operational transconductance amplifier (OTA), pipelined ADC , semidigital amplifier,HSPICE,FINFET.***

I. INTRODUCTION

THE PIPELINED analog-to-digital converter (ADC) has been widely adopted as an optimal architecture for medium-to-high resolution applications. To meet application specific requirements, research on the pipelined ADC has been mainly driven for the design of a high-speed, low power, and high-gain operational amplifier (op-amp). Due to their high immunity to short channel effects, importance of MOSFET with multiple gates (MUGFET) or FinFET's are increased by technologists for sub-100nm [1]. Especially for the digital applications, numerous FinFET realizations have reported with effective and improved feasibility, economy and performance with respect to up to date CMOS bulk technologies [2, 3, 6, 8]. Since, the FinFETs have better electrostatic channel control characteristic with improved turn off, they are considered as promising candidate for the future's fulfilling CMOS device demands [2]. In addition to excellent channel control, the FinFET transistors also offer approximately twice the on-current because of the two channels, even without channel doping. This is beneficial for the carrier mobility and results in a low gate leakage at the same time [7]. Correlated shifting (CLS) [6] and split-CLS [7] architectures have been also proposed for a high effective gain with low-gain amplifiers.

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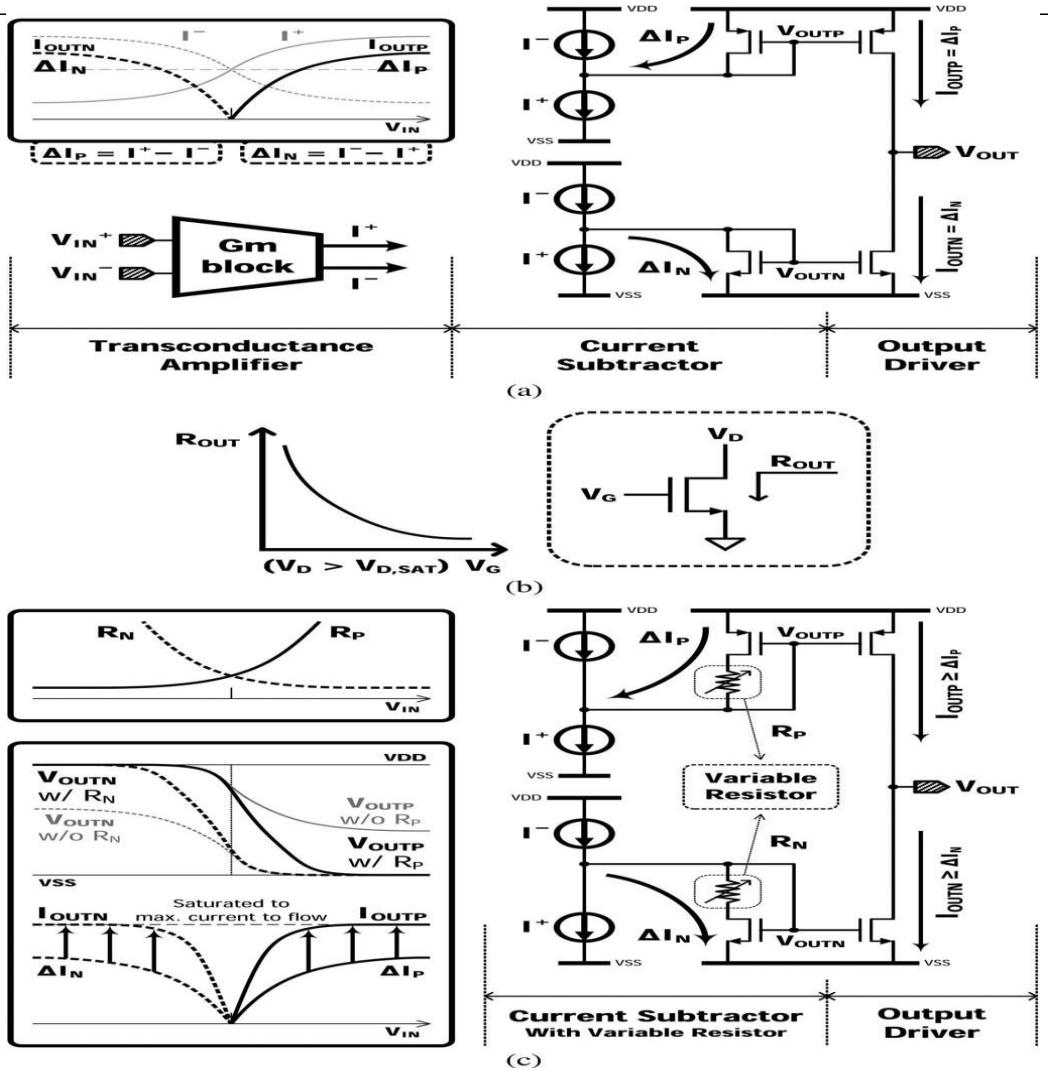

Fig. 1. (a) Concept of the Gm-based amplifier (b) Characteristic of the output resistance of MOSFET. (c) Operation of the variable resistor.

However, the use of an extra phase still presents a trade off limitation among gain, speed, and power consumption.

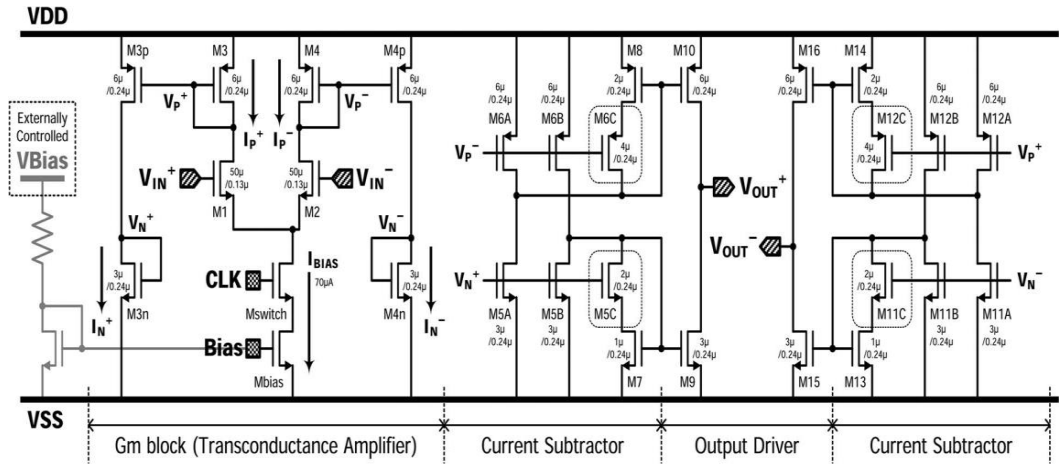

Fig. 2. Schematic of the semidigital Gm based amplifier

This brief presents a low-power pipelined ADC using a Gm-based amplifier that follows a conventional two-phase switched-capacitor circuit. Without any calibration technique or digital control, the proposed amplifier achieves a smooth transition from a comparator-like semi digital operation to a continuous-time high-gain amplifier whenever needed.

The Concept of device scaling has been consistently endorsed over the past few decades in meeting performance and power consumption requirements in VLSI circuits. Scaling to 45 nm node and below might necessitate the use of new processing steps or new device concepts such as FinFETs. High-performance SOI CMOS circuits, compatible with low-power low-voltage (LP/LV) and high-speed, ultra-large-scale-integration (ULSI) applications, have been repeatedly demonstrated on submicron devices.

The amplifier performs a class-AB operation by smoothly changing between a comparator-like semi-digital driver and a continuous– time high-gain amplifier according to the input voltage difference. A 10-bit pipelined ADC with 2.5-bit/stage architecture is implemented in a 0.45-μm CMOS.

II. SEMIDIGITAL GM-BASED AMPLIFIER

Fig. 2 shows the concept of the Gm-based amplifier,which is comprised of a Gm block, a current subtractor stage, and an output driver stage. The amplifier gain is the product of Gm and the output resistance of the output stage. While Gm does not change much by bias control, the output resistance of a transistor significantly increases as the gate-to-source bias decreases. If the transistors in the output driver are biased to operate in deep-subthreshold region, which almost turns the transistors off, the output resistance approaches to infinity, resulting in an infinite gain of the amplifier . To operate the output transistors in deep-subthreshold region for high gain, the output stage should be biased to flow the least current. It is provided by the Gm block followed by the current subtractor stage. As differential input voltage, i.e., V +IN− V−IN,approaches to zero, the output-biasing currents, i.e., ΔIP and ΔIN, become zero.In a practical device, the short-channel effect introduces an error in current subtraction. This nonzero error induces finite dc through the output transistors although the differential input voltage is zero. This limits the maximum output resistance. To suppress this error for higher gain, the bias current, i.e., IBIAS ,should be also small. However, it also reduces the driving current when needed.

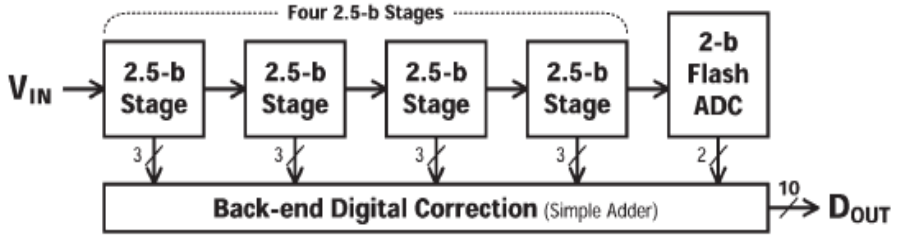

Fig 3.top block diagram of 10-bit ADC

In this case, this transistor tends to operate in the saturation region and drives a large swing. On the other hand, the transistor goes into the linear region as less current flows through it. Fig. 2 shows the detailed circuit schematic of the amplifier. M5C, M6C, M11C, and M12C function as variable resistors. The biasing of the output transistors in deep-subthreshold region gives additional benefits.Since the resistance of the output transistors and the load capacitance are much larger than the resistance of the current sources and the parasitic capacitance in the current subtractor, there is no need for an additional frequency compensation scheme.

Therefore, there is a tradeoff limitation between gain and speed performance. To alleviate this tradeoff problem, an extra variable resistor is inserted between the drain and gate nodes of the output-biasing transistor in the current subtractor while keeping *I*BIAS to a small value for high dc gain. Fig. 1(c) graphically illustrates the effect of the variable resistor, which boosts the output current whenever needed. The variable resistor is assumed to increase the resistance to the amount of the current flowing through it. As the differential input voltage increases, this resistance induces an even larger voltage drop.

III PROPOSED WORK

The proposed framework is designing a op-amp comparator which can be implemented in Finfet technology.

A. OTA

An operational transconductance amplifier (OTA) is a voltage controlled current source. One of the first papers on OTA in the literature appeared nearly 38 years ago. This paper described a bipolar OTA. At that time the emphasis was on amplifiers with feedback, such as opamps. In many analog or mixed VLSI applications, an operational amplifier may not be appropriate to use for an active element. For example, when designing integrated high-frequency active filter circuitry, a much simpler building block, called an OTA, is often used. More specifically the term "operational" comes from the fact that it takes the difference of two voltages as the input for the current conversion. The ideal transfer characteristic is given below in equation (1) and (2).

Iout =Gm(Vin+ Vin-) ……. (1)
Iout=GmVm ……..(2)

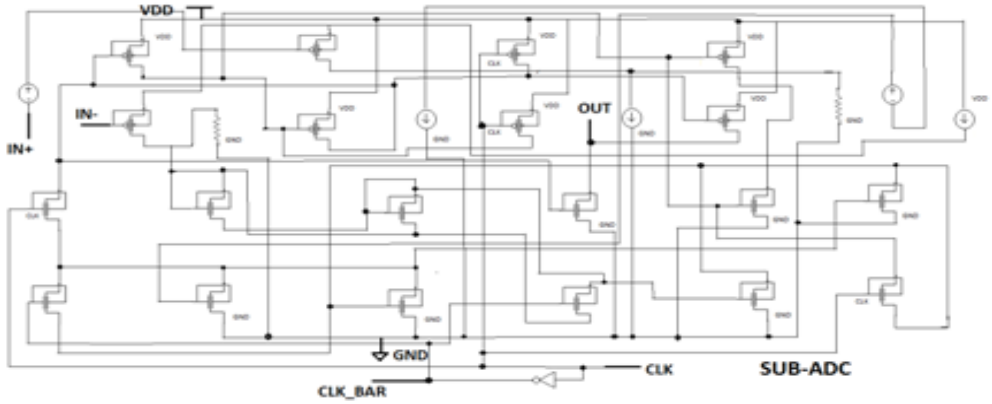

Fig 4. Schematic of the OTA .

SOI circuits consist of single-device islands dielectrically isolated from each other and from the underlying substrate . The lateral isolation offers more compact design and simplified technology than in bulk silicon, since there is no need of wells or interdevice trenches. On the other hand, the vertical isolation allows erasing of the word latch-up from the SOI dictionary [10]. For low off-current, bulk MOS-devices need sufficiently high channel doping, which degrades the carrier mobility. Moreover, good channel control and high on current demand for a thin gate dielectric. However, especially for low power applications, the gate leakage current through thermal oxide becomes unaccepted high for thicknesses approaching 2 nm. Therefore a nitride oxide or even a high-k-dielectric is required, which up to now suffers from reduced carrier mobility with respect to thermal oxide [2]..

In such technologies, one can choose to connect the back and front gates together or to control them separately while designing a circuit resulting in new circuit styles. Connected back and front gates 3-T provides a simple way of mapping circuits designed in single gate technologies to double gates technologies. 3-T configuration provides more ON current for transistors as well [8].

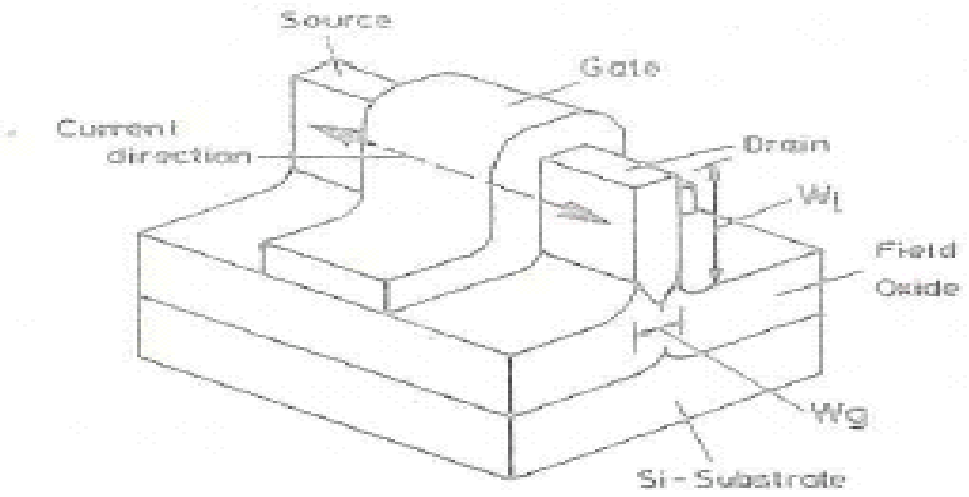

Fig. 6. Top view of Finfet Technology.

B. DIBL

Barrier lowering increases as channel length is reduced, even at zero applied drain bias, because the source and drain form pn junction with the body, and so have associated built-in depletion layers associated with them that become significant partners in charge balance at short channel lengths, even with no reverse bias applied to increase depletion width.In addition, the proposed amplifier does not require common-mode feedback when used in switched-capacitor circuits driven by nonoverlapping two-phase clocks [1]. In the beginning of output transition,the current subtractor differentially drives the output. After the settling is completed, the output voltage hardly drifts due to the negligible output current in steady state, as explained in [1]. In this brief, the bias current of the Gm block in the first multiplying digital-to-analog converter (MDAC) stage is designed to be 40 μA. The steady-state current through the output driver is around 2−3 μA. The designed amplifier has a unity-gain bandwidth of 260

MHz with a 58◦ phase margin (see Fig. 5). For comparison, the case of the conventional operational transconductance amplifier (OTA) without the current subtractor is also added in the same figure. Monte Carlo simulations show a stable dc gain of more than 65 dB (see Fig. 4). In this simulation, we gave 5% mismatches to the width of transistors in the current subtractor with a • 3 − σ variation (99.7% coverage). The current and voltage transients, except *V*OUT, are plotted in a single-ended manner for a clear view. The settling time is improved from 30 to 18 ns by variable resistors without any increase in current consumption. The current subtractor acts as a comparator in the beginning of the transition where the output transistors are fully driven to conduct the maximum current. Thus, the operation is almost digital as in the comparator-based approach [1] in the beginning, but it is smoothly shifted to fine settling mode as the input difference decreases.

IV. IMPLEMENTATION RESULT

A 10-bit pipelined ADC (see Fig. 4) is taken to verify operation of the proposed amplifier. A sample-and-hold amplifier (SHA)-less architecture [8] is chosen with a general architecture of four stages of 2.5-bit MDAC followed by a 2-bit Flash ADC. The total input capacitance of the first stage is approximately 4.5 pF. For the second, third, and fourth stages, the unit capacitance and the bias current are scaled down to 75% and 45%, respectively. Bootstrapped switches are employed for input sampling in the first stage. The 2.5-bit sub-ADC is comprised of six comparators (see Fig. 5). Each reference voltage is tapped from a resistor ladder. The unit capacitance in the sub-ADC is 83 fF.

The designed ADC was fabricated in a 0.45-μm CMOS . The active area is 0.9 mm2. The maximum sampling rate was 25 MS/s with 1-V supply voltage. Measured differential nonlinearity (DNL) and integrated nonlinearity (INL) are +0.35/ − 0.23 LSB and +0.4/ − 0.68 LSB, respectively (see Fig. 6). Fig. 10 shows fast Fourier transform (FFT) spectra with normalized 0-dB input sinusoids at 27 KHz and 10.7 MHz, respectively. The spurious-free dynamic range (SFDR) and the signal-to-noise and distortion ratio (SNDR) are 67.9 and 57.5 dB at low frequency, showing an effective number of bits (ENOB) of 9.27. The SFDR and the SNDR drops by 10 and 4.6 dB at 10.7 MHz. The total power consumption is 1.25 mW excluding the dc through the resistor ladder in the 2.5-bit sub-ADCs, consuming 840 μW, which was not considered for optimization since this design was mainly focused on opamp design. The calculated figure-of-merit (FOM) is 139 and 232 fJ/c-s without

and with including the dc power consumption from the resistor ladder. The power consumption from the total four amplifier circuits is measured to be only 395 μW.The ADC was designed to operate at 50 MS/s in a 1.8 V, 130nm CMOS process.

V. CONCLUSION

Class-AB amplifiers have been generally considered in lowpower switched-capacitor circuits since they reduce static current without complicated digital control. However, as supply voltage decreases, the class-AB schemes do not give significant benefit both in speed and power consumption. The OTA circuit operated in a limited range.This is just a start of the FinFET based analog integrated circuit design. The high frequency range of the OTA circuits show that the FinFET SOI is a future candidate of current bulk CMOS technology. The proposed OTA circuit requires more improvements for the future works. Although this situation, the realization proves that the SOI FinFET technology can easily replace the circuits of current bulk MOS technology.

REFERENCES

[1] I. Ahmed, J. Mulder, and D. A. Johns, “A low-power capacitive charge pump based pipelined ADC,” *IEEE J. Solid-State Circuit*, vol. 45, no. 5, pp. 1016–1027, May 2010.

[2] D.-Y. Chang, “Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 11, pp. 2123–2132, Nov. 2004.

[3] B.R. Gregoire and U.-K. Moon, “An over-60 dB true rail-to-rail performance using correlated level shifting and an op amp with only 30 dB loop gain,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2620–2630, Dec. 2008.

[4] J. Hu, N. Dolev, and B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-Mw pipelined ADC using dynamic source follower residue amplification," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1057–1066, Apr. 2009.

[5] D.-W. Jee, S.-J. Park, H.-J. Park, and J.-Y. Sim, "A low-voltage OP amp with digitally controlled algorithmic approximation," in *Proc. IEEE CICC*, 2008, pp. 499–502.

[6] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U. Moon, "A 61.5dB SNDR pipelined ADC using simple highly-scalable ring amplifiers," in *Proc. Symp. VLSI Circuits*, 2012, pp. 32–33.

[7] B. Hershberg, S. Weaver, and U.-K. Moon, "Design of a split-CLS pipelined ADC with full signal swing using an accurate but fractional signal swing opamp," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2623– 2633, Dec. 2010.

[8] P. Huang, S. Hsien, V. Lu, P. Wan, S.-C. Lee, W. Liu, B.-W. Chen, Y.-P. Lee, W.-T. Chen, T.-Y. Yang, G.-K. Ma, and Y. Chiu, "SHA-less pipelined ADC with in situ background clock-skew calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1893–1903, Aug. 2011.

[9]W. Rösner, E. Landgraf, J. Kretz, FinFETs for low power applications, Solid-State Electronics, Vol. 48, pp. 1819-1823, 2004

[10]. R. Zhang, K. Roy, Low-Power High-Performance
Double-Gate Fully Depleted SOI Circuit Design, IEEE Transaction on Electron Devicev, Vol. 49, No.5, pp. 852-861, 2002.

[11]. K. Kim, O. Kwon, J. Seo, Nano-scale Device Modeling and Simulation: FinFET, International Microprocesses and Nanotechnology Conference, pp.
24 - 25, 2003.

[12]. D. Fried, J.S. Duster, K.T. Kornegay, High- Performance P-Type Independent-Gate FinFETs, IEEE ELECTRON DEVICE LETTERS, VOL. 25, NO. 4, pp. 199-201, 2004.

[13]. R.V. Joshi, R.Q. Williams, E. Nowak, FinFET SRAM for High-Performance Low-Power Applications, Solid-State Device Research conference, pp.69-72, 2004

[14]. S. Cristoloueanu, SOI a metamorphosis of silicon,
IEEE Circuits & Devices, pp. 26-32, 1996.

[15]. A. Marshall, M. Kulkarni, M. Campise, R. Cleavelin, FinFET Current Mirror Design and Evaluation, Architecture,IEEE Dallas/CAS Workshop: Circuits and Implementation of SOCs, pp. 187- 190, 2005.