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Performance comparison of three phase five level and seven level DCMLI.

SagarUttamShinde[1] ,K. Vadirajacharya[2]
Electrical Engineering Department.
Dr.BabasahebAmbedkar Technological University, Lonere
Sagar.shinde78@gmail.com,kvadirajacharya@dbatu.ac.in

ABSTRACT—*Multilevel inverter technology has emerged as a very important alternative in the area of high-power medium-voltage energy control. It offer several advantages as compared to the hard-switched two-level pulse width modulation inverters, such as their capabilities to operate at high voltage with lower dv/dt per switching, high efficiency, low electromagnetic interference. The THD and switching losses will vary with respect to topology and control technique adopted. This paper aims at comparing the performance of three phase five and seven level diode clamped inverter with respect to their THD, switching losses and number of components. The performance is verified through extensive simulations on MATLAB Simulink platform for IGBT device.*

Keywords— high-power medium-voltage energy control, THD, FFT Analysis, 5 & 7 level diode clamped MLI.

1. INTRODUCTION

A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multilevel inverter is their small output voltage, results in higher output quality, lower harmonic component, better electromagnetic computability, and lower switching losses.

Multilevel inverters also have interest in the field of high-voltage high-power applications such as compressors, mills, conveyors. The most familiar power circuit topology for multilevel converters is based on the neutral clamped multilevel inverter. The key issue in designing an effective multilevel inverter is to ensure that the total harmonic distortion (THD) of the output voltage waveform is within acceptable limits.

For high switching frequency classified as space vector PWM, Selective Harmonics Elimination PWM and SPWM. Among these PWM methods SPWM is the most used for the multilevel inverter, because it has very simple and easy to implemented. In this paper present

SPWM method with comparison of the five & seven level diode/neutral point clamped multilevel inverter has been analyzed.

2,DIODE CLAMPED MULTILEVEL INVERTER TOPOLOGIES

The Diode clamped multilevel proposed by Nabae, Takashi, and Akagi in 1981 was named as neutral point converter and was essentially a three-level diode clamped inverter as shown in fig.1.

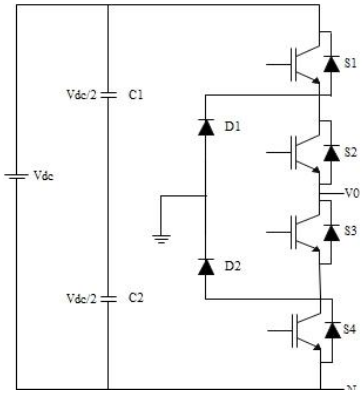

Fig.1. Three level DC-MLI

Table 1: Voltage levels of seven-level DC-MLI and switching states.

Van	Switching state											
	Sa_1	Sa_2	Sa_3	Sa_4	Sa_5	Sa_6	Sa_1^1	Sa_2^1	Sa_3^1	Sa_4^1	Sa_5^1	Sa_6^1
$V_6 = V_{dc}/2$	1	1	1	1	1	1	0	0	0	0	0	0
$V_5 = V_{dc}/4$	0	1	1	1	1	1	1	0	0	0	0	0
$V_4 = V_{dc}/6$	0	0	1	1	1	1	1	1	0	0	0	0
$V_3 = 0$	0	0	0	1	1	1	1	1	1	0	0	0
$V_2 = -V_{dc}/6$	0	0	0	0	1	1	1	1	1	1	0	0
$V1 = -V_{dc}/4$	0	0	0	0	0	1	1	1	1	1	1	0
$V_0 = -V_{dc}/2$	0	0	0	0	0	0	1	1	1	1	1	1

Each of the three-phase outputs of inverter shares a common DC bus voltage that has been divided into seven levels over six DC bus capacitors. The capacitors have been subscripted from C_1 to C_6. The middle point of C_3 and C_4capacitors constitute the neutral point of inverter and output voltages have seven voltage states referring to neutral point. The voltage across each capacitor is $V_{dc}/6$ and the voltage stress on each switching device is limited to V_{dc} through the clamping diodes that have been named as $D_{1.6}$ and $D_1^1.{}_6^1$. The key components that differ with this topology from a conventional two-level inverter are clamping diodes. To

explain how the staircase voltage is synthesized, the neutral point n has been assumed as the output phase voltage reference and the switching combinations have been analyzed for phase A output voltage Van as seen in table.1.

For the seven-level DC-MLI in fig.1, a set of six switches is ON at any given period of time and they are S_{a1} to S_{a6} for voltage level of Van=V_{dc}/2. The second switching states that constitutes 0 and negative outputs can be seen in table 1. The clamping diodes require different voltage ratings for reverse voltage-blocking due to each triggered switch is only required to block a voltage level of V_{dc}/(n-1). By assuming the switches from Sa_1 to Sa_6 are triggered as seen in first line of table 1, D_1 blocking diode needs to block a voltage at the rate of $5V_{dc}$/6 that is generated by three DC bus capacitors. Since each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be calculated as (n-1).(n-2), where n represents number of inverter levels.

The following equations are used to determine the required device numbers to form a given level of a diode/neutral point clamped MLI[3]. If n is assumed as the number of levels, the number of capacitors at the DC (c) side can be known by using equation (1). If d is the number of freewheeling diodes per phase, and d_c is the number of clamping diodes (2) & (3) respectively. Then,

$$C = n-1 \quad (1)$$

$$d = 2(n-1) \quad (2)$$

$$d_c = (n-1).(n-2) \quad (3)$$

In the DC-MLI the number of increasing levels directly depends on the number of increasing clamping diodes which makes topology complex[1][2].

3. 2.CARRIER BASED DISOPOSITION PWM METHOD

Carrier based disposition PWM methods were first proposed by Carrara et al[3]. For an *n*-level inverter, *n*-1 carriers with the same frequency $f_c$and the same amplitude $A_c$are disposed such that the bands they occupy are contiguous. The reference waveform has maximum amplitude A_m, a frequency f_m, and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the IGBT corresponding to that carrier is switched on and if the reference is less than a carrier signal, then the IGBT corresponding to that carrier is switched off [4]. Previous works on PWM techniques shows that disposition technique for diode clamped and PSCPWM for cascaded inverter five rises to same harmonic profile for the

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same number of total switch transition. Hence these techniques can be efficiently applied for Diode Clamped and Cascaded Multilevel Inverter.

Carrier Disposition method arrange n-1 carrier waveform of same amplitude and frequency in continuous bands to fully occupy the linear modulation range of the inverter. The reference or modulating wave is positioned at the center of the carrier set, and continuously compared with the carriers to obtain the necessary gating pulses [4].

In multilevel inverters, the amplitude modulation index (M.I.) is the ratio of reference amplitude (R_a) to carrier amplitude (C_a).

$$M.I. = R_a / (m-1)C_a \quad (4)$$

The frequency ratio (R_f) is ratio of carrier frequency (f_c) to reference frequency (f_r).

$$R_f = F_c/F_r. \quad (5)$$

4, SIMULATION RESULTS

The SPWM for the three-phase five level& seven level multilevel inverter is implemented on a MATLAB SIMULINK model, out of which the seven level DC-MLI is shown below. The simulated results for five & seven level are compared for different modulation indexes with the input voltage 600V.

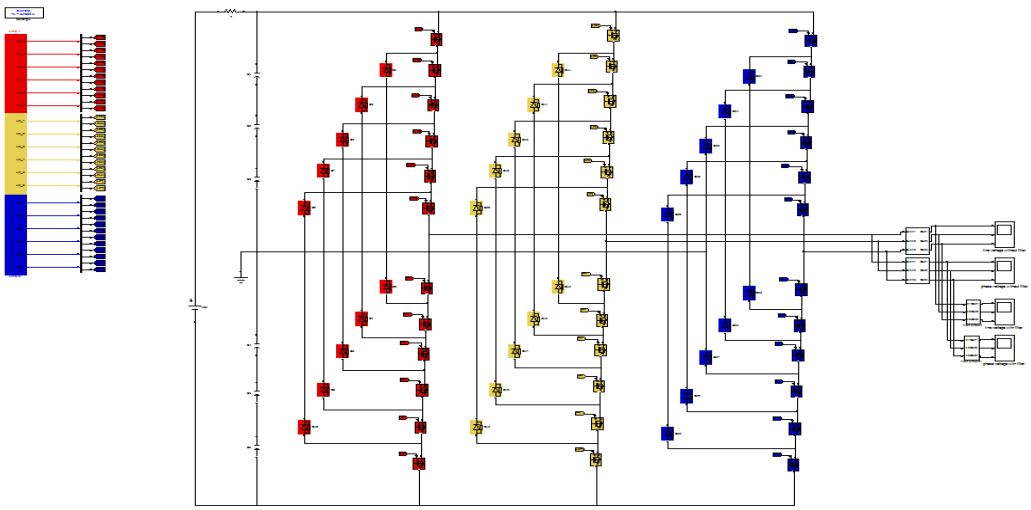

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Fig. 2. Simulation diagram of the seven level diode clamped multilevel inverter.

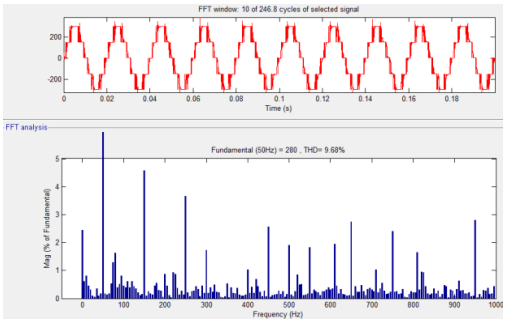

Fig. 3.Five level Line to ground without filter

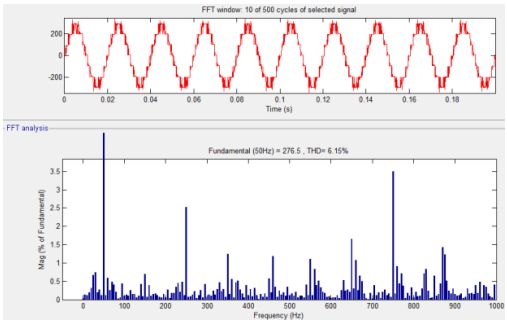

Fig. 4. Seven level Line to ground voltage without filter

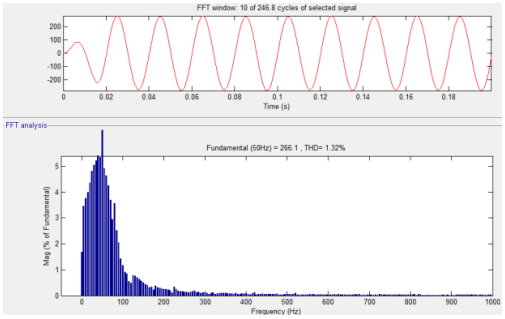

Fig.5. Five level Line to ground voltage with filter

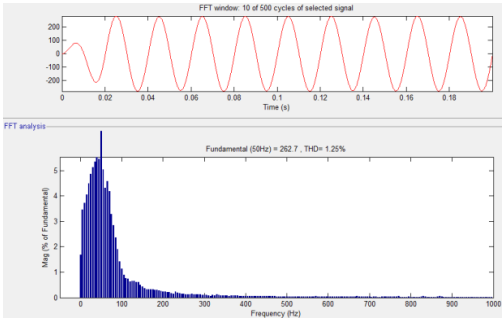

Fig. 6.Seven level Line to ground voltage with filter

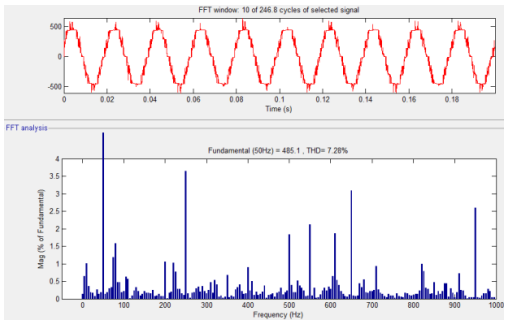

Fig. 7. Five level line to line voltage without filter

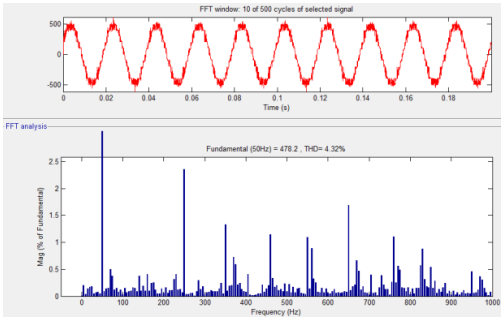

Fig. 8. Seven level line to line voltage

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without filter

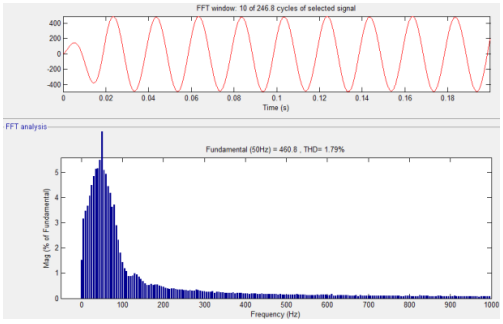

Fig.9. Five level line to line voltage with filter

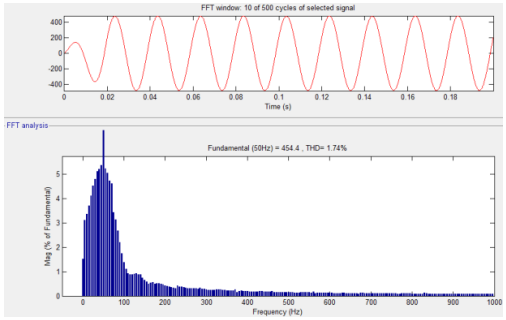

Fig.10. Seven level line to line voltage with filter

Table 2: Output voltages & %THD for different modulation index

Level	5 level				7 level			
M.I.	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
V_o without filter	166	207	234	280	188	208	242	268
THD (%)	15.3	14	10	9.7	8.5	7.6	8.2	6.2
V_o with filter	158	197	223	266	179	198	230	268
THD (%)	1.2	1.3	1.2	1.3	1.3	1.2	8.3	1.3

5, CONCULSION

The SPWM control strategy method for the five and seven level diode clamped multilevel inverter has been presented in this paper. As we goes on increasing the level of the multilevel inverter the dv/dt rating of the switches decreases, it reducing the cost per component, the number of component increases, complexity increases. As we increase the modulation index the output voltage increases & the %THD reduced.

6, REFERENCES

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