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A Novel Approach for Low-EMI and UPF Uninterruptible Power Supply

R.Dhanasekaran   and   M.Murugan
Research Scholar   Post Graduate Student

Department of Electrical and Electronics,
Government College of Technology, Anna University,
Coimbatore-641 013,Tamil Nadu, INDIA
tamizh_kavi@yahoo.co.in and rdhanashekar@yahoo.com

*A*bstract

A novel line interactive UPS configuration is investigated that offers the characteristics of an on-line or inverter preferred UPS that features low-EMI and draws Unity Power Factor (UPF) without the addition of a pre-regulator at a reduced cost. This new UPS is based on combination of two full bridge VSI converters, one series with the input, and other parallel to the load. The UPS acts as a line conditional and output voltage stabilizer. The series converter sees only a small percentage of the input voltage. Therefore small kVA rating, which results reduced system cost compared conventional on-line system cost compared conventional on-line system and a new high frequency dc-dc converter is proposed, which is based on a half bridge series resonant converter. The converter features Zero Voltage turn on, snubbed turn off at reduced current for the switching device and operating at switching frequency higher than 20kHz. The efficiency of the converter is very high under full load and low load conditions, so total component converter structure exhibits high efficiency.

Index Terms-- UPS, ZCS, ZVS, EMI .

I. INTRODUCTION

On-line UPS find wide applications today, in critical loads like computer, hospitals and airline reservation system need Uninterruptible Power Supply. UPS provide

protection against power outage as well as voltage regulation during power line over voltage and under voltage condition. However it may generate EMI and input power factor can be very poor. EMI is the

degradation in the performance of a device, or equipment caused by an electromagnetic disturbance. Power factor also has another serious and undesirable effect on the power supply. Therefore we have to reduce EMI and improve the power factor is important. Traditionally quick solutions to EMI and low power factor have been brought about by introducing filters and pre-regulator to existing equipment [1]. This had the effect of increasing the cost of the system and output link voltage making reduction of EMI even more difficult. This thesis describes a UPS topology specifically structured to have both Unity Power Factor and Low- Electro Magnetic Interference. The design is based on the principle of Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS) as well as incorporating internal waveform shaping modules.

Fig.1 shows the block diagram of a

typical unity power factor On-line UPS with galvanic isolation. The design includes a pre-regulator on the input after the mains rectifier, which shapes the current waveform by high frequency modulation to obtain Unity Power Factor. In the process, the rectified input voltage is converted to a dc voltage. This dc voltage is inverted to a high frequency transformer, which also provides galvanic isolation. The secondary voltage is rectified to charge the battery and supply the output dc link voltage. This voltage is inverted by a pulse-width modulation inverter to supply 230V at 50Hz, to the load.
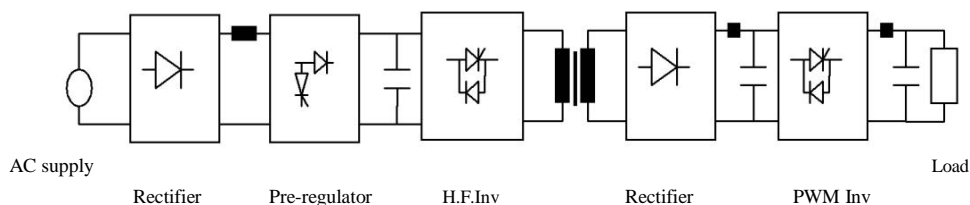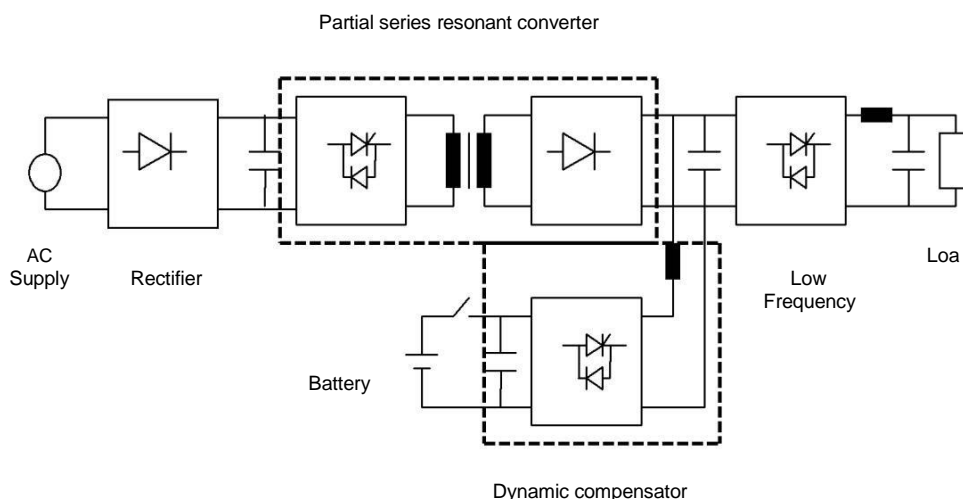
Fig.1.Block Diagram of Conventional UPS

Fig. 2. Block Diagram of proposed UPS

One disadvantage of such a system is the high dc output voltage of the pre-regulator and from where the rest of the system must operate. The hard switching nature of the boost converter also has the tendency to aggravate conducted EMI to the supply. The typical transformer that is used has an appreciable inter-winding capacitance, thus allowing EMI generated by the output inverter and the load to coactively couple to the mains supply. Another drawback of this approach is the dual filters that are required for the system's output and input. Any new design must address some or all of these disadvantages.

II.SYSTEM DESCRIBTION

Fig.2 shows the block diagram of the low EMI and UPF UPS. Input rectifier rectifies

the main input voltage to dc voltage. Then a dc-to- dc converter, the Partial Series Resonant Converter (PSRC) [2], to a high frequency ac voltage, which passes through a transformer to provide galvanic isolation, inverts the dc voltage. The pulsed dc voltage is inverted to 50Hz, 230V ac by a low frequency inverter that supplies the load. Any reactive power from the load is absorbed by a bi-directional dc-to-dc converter connected in parallel to the capacitor (C_4), which acts as a compensator and with typical voltage and current waveform. The second function of this bi-directional inverter is to charge the battery and, in the event of a mains failure, to provide power for the load. This converter will be referred to as "dynamic compensator".
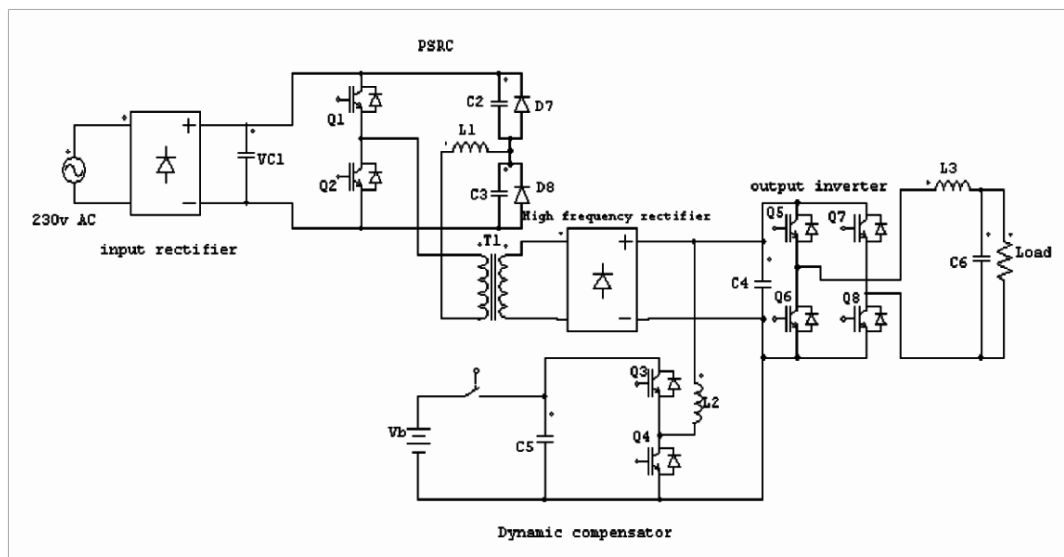
Fig.3 Power Circuit of Low EMI & UPF UPS

III.POWER CIRCUIT AND OPERATION

The power circuit consists following four main sections:

1. An input rectifier
2. A dc-to-dc ZCS-PSRC, including the high frequency rectifier
3. A dynamic compensator
4. An output rectifier

A. Input Rectifier

The input rectifier converts the 230V, 50 Hz ac voltages to a pulsating DC voltage of 100Hz. This is achieved by small capacitor (C_1) after the diode bridge, which is typically 1μF.

B.Partial Series Resonant Converter

PSRC is a soft switching partial resonant dc-to-dc converter. It is a half bridge series resonant converter, which is having only two switches, and resonance occurs only for a part of each cycle and a

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discrete energy pulse is transferred to the transformer every half cycle, rendering a variable frequency controller controlling the output power of the PSRC, and its ability to draw only positive generating current pulses from the capacitor (C_1). This allows the use of a very small capacitance on the input, which translates to an improved power factor.

A transformer can be included to provide the output voltage of desired magnitude as well as the electrical isolation between input and output. The transformer of the PSRC can be constructed in such a way to exhibit a very low inter-winding capacitance. This is done by winding the primary and secondary windings in such manner that a complete air-gap is formed between these two windings. This feature traps conducted EMI generated by the output inverter, dynamic compensator, and even the load connected to the output of the UPS. The air-gap produces a series inductance that forms part of the circuit. The PSRC converter itself does not generate excessive EMI, due to slow dv/dt's and small commutation currents [3].

C. Dynamic Compensator

This converter has several functions, namely the following

1. The converter manages the reactive power that the load may generate by compensating for the load current drawn by output inverter to the current drawn by the PSRC.
2. It delivers active power in the event of a mains failure, from the battery connected at capacitor (C_5). It then operates as a buck converter modulated by a full wave rectified sine wave.
3. During the ON periods, the additional energy is used to charge the capacitor (C_5), and during the OFF periods, it is used to continue to supply energy to the load.
4. The converter charges the battery placed across the capacitor (C_5) when operating as a boost converter, by drawing energy from the PSRC in such a manner as to maintain unity power factor on the mains supply.

The dynamic compensator is the only hard switching topology in the circuit. This is due to the difficulty in designing a steady state interface between ac and dc voltages using soft switching techniques. The converter is a bi -directional half bridge dc-to-dc converter made up of a combination of a buck converter with capacitor (C_5) as its source and a boost converter with capacitor (C_4) as its source. If the switches cannot conduct as a result of current flow direction, the corresponding diode will conduct. The battery can be charged or brought into function by means of an additional switch. The UPS requires a battery voltage higher than the peak line voltage in this configuration. This can be achieved by using a high voltage battery followed by an additional dc-to-dc converter to step up the voltage.

D. Output Inverter

The function of this converter is to invert the 100Hz pulsated dc voltage to a sinusoidal ac voltage of 230V, 50Hz. It switches at 50Hz under zero voltage

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conditions without the need for resonant components or snubbers, ensuring high efficiency. It is also possible to use slow switches with a low on-state voltage drop, thus keeping conduction losses to a minimum. During the resonant current reversal period, the inverter effectively disconnects the load from the voltage across the capacitor (C_4) by turning Q_5 and Q_7 ON or, alternatively, Q_6 and Q_8, and maintains the current flow through the load.

IV. CONVERTER ANALYSIS

The UPS is comprised of three controlled sub converter. The switching and the operation of the sub converters are explained in this section.

A .PSRC

The voltage limit across the resonant capacitors which is introduced by D_7 and D_8, also limits the voltage stresses, which is an important improvement regarding cost and reliability, especially at high power levels.

Energy stored in the resonant capacitors is given by

$$E_c = \frac{1}{2} C_r V_{c1}^2 (t) \qquad (1)$$

When some of the energy contained in C_2 and C_3 is fed back to the supply, that is commutation of the phase arm before the entire energy pulse is transferred to the output, will not be valid, and a larger switching frequency for a given output power will be obtained and is transferred to output during each half switching [3,6]. This result in the output power of the PSRC is

given by

$$P_{out}() = E_c .2 f$$

$$P_{out}(t) = C_r .V_{c1}^2(t) .f \qquad (2)$$

For power level below a certain level, the converter is periodically turned ON and OFF in bursts or multiplies, hence burst control, of the 50Hz mains supply, maintaining full sinusoidal cycles of the 50Hz mains voltage during the ON and OFF

periods. This is ensuring minimum harmonic distortions of the line current drawn from the mains supply and, thus, maintains a high power factor. Since the power level is low, it should not play an important role on the flicker value it would generate. The voltage limit across the resonant capacitors which is introduced by D_7 and D_8, also limits the voltage stresses, which is an important improvement regarding cost and reliability, especially at high power levels.

B.Dynamic Compensator

The operation of the dynamic compensator is comprised of two functions, namely, current compensation and the resonant current reversal.

1.Current Reversal

In this mode, the current flows in the inductor L_2 during the positive and negative half cycles and the compensating current is given by

$$i_{comp}(t) = i_{PSRC}(t) - i_{ld}(t) \qquad (3)$$

For this discussion, the high frequency ripple caused by the PSRC and the phase arm of the dynamic compensator is averaged out, so as to exclude the effects of the high frequency ripple. This compensating current $I_{comp}(t)$ flows in the inductor. Due to the nature of the output inverter, this current is discontinuous whenever the output voltage passes through zero. The current amplitude remains constant, but the polarity reverses.

2 Resonant Current Reversal

In case of a reactive or non linear load, the load current $I_{load}(t)$ will not be equal to zero during a voltage zero crossing. When the load produces a reactive current, the currents during mains zero voltage crossing. Therefore the compensating current $I_{comp}(t)$ will change abruptly from

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positive to negative. One method to reverse this current is by means of a resonant cycle. This is achieved by a careful choice of C_4 and L_2, the main criteria being the allowable voltage overshoots across C_4, as the value for C_4 is fixed to the allowable ripple voltage of the converters during normal operation.

The value of the output capacitor C_4 determines the main value of the voltage ripple. There are two sources for the ripple voltage, firstly, the PSRC and secondly, the dynamic compensator. The value of C_4 is given by

$$C_4 = \frac{Q_{PSRC} + Q_{COMP}}{\Delta V_{C4}} \qquad (4)$$

The voltage across C_4 during the resonant period is given by

$$VC_4(t) = I_{trans.}\sqrt{\frac{L^2}{C_4}}.Sin(\frac{t}{\sqrt{L_{2.}C_4}}) \qquad (5)$$

The peak voltage overshoots during the resonant period id given by

$$VC_4 = I_{trans}\sqrt{\frac{L_2}{C_4}} \qquad (6)$$

and the current in the inductor L_2 during the resonant phase arm is given by

$$I_{comp}(t) = I_{trans}.COS(\frac{t}{L_2.C_4}) \qquad (7)$$

the resonant period is given by

$$t = \pi \underline{\qquad\qquad}$$

$$\sqrt{}$$

$$\sqrt{L_2 C_4} \qquad (8)$$

The current reversal period is small (typically 4% of a 50Hz) and contributes very little to the total harmonic distortion on the mains supply current. The dead time of the input current is as a result of a current reversal in the dynamic compensator. The dynamic compensator used not only results

in cost savings, but also results in an improved dynamic response of the UPS as the load changes

C.Output Inverter

The inverter is fed by a 100Hz pulsed DC voltage V_{C4}. The inverter switches at 50Hz, alternatively switching the diagonal pairs Q_5 and Q_8 ON while Q_6 and Q_7 remain OFF for the positive cycle and vice versa for the negative cycle. The switching occurs at the zero voltage crossing of the mains supply, thereby reconstructing the sinusoidal voltage that will be supplied to the load. During resonant reversal period, switches Q_6 and Q_8 are turned ON, while Q_5 and Q_7 remain OFF. This allows for the inductor current $I_{comp}(t)$ to be reversed and the load current to continue flowing. Output filtering comprised of L_3 and C_6 filters out the high frequency on C_4 and smooth out the zero crossing transition on the output voltage [7]. The filtered output of the inverter is very low harmonic distortion, even though most loads are highly nonlinear and, hence, inject larger harmonic currents into the UPS. The output voltage harmonic content is specified by means of a term called Total Harmonic Distortion (THD), which was defined by

$$\% \, THD \;=\; 100 \;\cdot\; \frac{\sum_{h=2}^{\infty} V_h^{\,2}}{V_1}$$

Typically, THD is specified to be less than 5%; each harmonic voltage as a ratio of V_1 is specified to be less than 3% [8].

V.CONTROL AND OPERATION

The frequency of the PSRC is varied to control the output power of the converter. The switching frequency of the PSRC is kept constant within a 50Hz cycle, so as not to cause harmonic distortion of the current waveform drawn from the main supply.

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Equation (2) shows that the output power of the PSRC is proportional to the switching frequency. As the switching frequency is increased and, if the output voltage remains relatively constant, the current drawn from the supply will also increase. As a result, the power delivered to the load will also increase. Therefore, if during a 50Hz cycle the switching frequency changed, then the input current will change proportional to the switching frequency, thus producing a current distortion. The switching frequency can thus be modulated, to further improve power factor and current wave shapes.

The controller circuit is used to maintain constant voltage across the capacitor C_5, which is across the battery. The voltage VC_5 across C_5 is measured and, if it rises above a certain level, then the controller cuts back the frequency of the PSRC. If the voltage drops below a certain level, then the controller increases the frequency of the PSRC, therefore output power of the PSRC is changed, so this change in power will ultimately control the changes in V_{C5}, thus maintaining a relatively constant voltage across C_5.

During a power failure, the operation of the system changes. The dynamic compensator now has to deliver power to the load. The PSRC is no longer in operation, and the voltage-controlled oscillator, therefore, shutdown in order to ensure a soft start upon the mains supply being restored. The system reduces to that of a step down converter sourced by the battery placed across C_5. The controller operates in the same manner as in normal conditions and will still maintain the voltage waveform V_{C4} across C_4, thereby retaining the pulsed

voltage. This ensures low output EMI, even during mains failure conditions.

VI.SIMULATION AND RESULTS

The design parameter values of the above circuit are
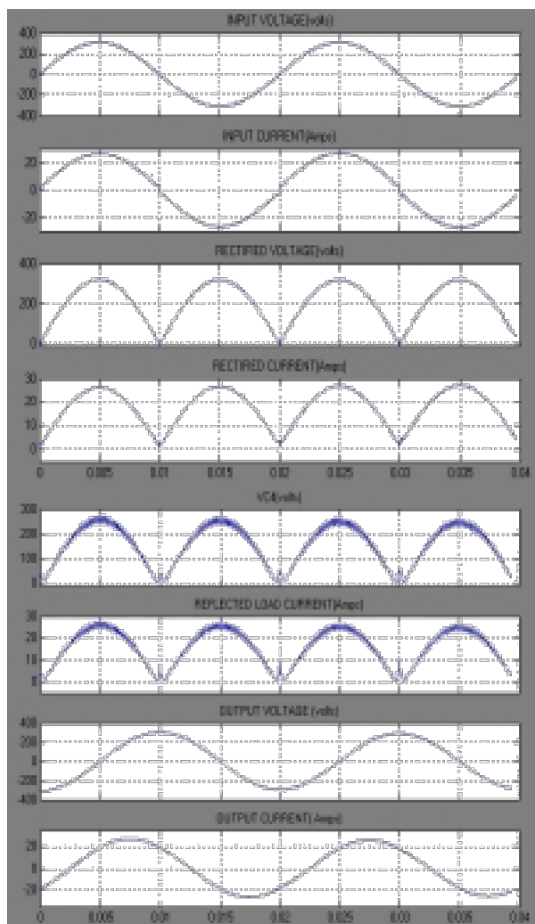
$C_1 = 1\mu F$
$C_2 = 220nF$
$C_3 = 220nF$

waveform of the main circuit at supply ON condition.

From the results it has been inferred that, power factor is 0.994, and conducted EMI is very less, and the efficiency is calculate from following measures, the input voltage, current and power are as follows

Fig.4 Input and Output waveforms for proposed UPS

$$C_4 = 43\mu F$$
$$L_1 = 6.1\mu H$$
$$L_2 = 88\mu H$$

The resultant waveforms of the above circuit have been simulated and have been given in figure4. Fig.4 shows the resultant

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V_{in} = 229.8 V
I_{in} = 17.78 A
P_{in}= 4080 W

The output voltage, current and power are as follows:

V_{load}=208 V
I_{load}=19.1 A
P_{load}=3950 W

The efficiency of the entire system under normal operating conditions is measured as 96.2%.

VII. CONCLUSION

A new UPS configuration has been described that features unity power factor, transformer isolation through a high-frequency link in the circuit. The concept was developed for generating lower conducted EMI, not only due to soft switching, but containing the frequency content of switching waveforms, particularly those closed to the input and output of the UPS. A single phase 230V, 50Hz, simulated circuit, load up to 3.2kW, has been presented, and measurements indicate the low EMI is possible, and a Power Factor of 0.996 was measured, by simulated waveforms in MATLAB software

NOMENCLATURE

$P_{out}(t)$ - output power of the PSRC in watt
f - operating frequency of the PSRC in Hertz
C_r - resonant capacitors (C_2+C_3) in Farads
$V_{c1}(t)$ - input across C_1 in volts.

$I_{PSRC}(t)$ - output current of the PSRC in

Amps
$I_{ld}(t)$ - reflected load current in Amps
$I_{comp}(t)$ - compensation current in Amps
Q_{PSRC} -- charge of PSRC into C_4 (C)
Q_{COMP} -- charge of dynamic compensator
ΔVc_4 -- maximum output voltage ripple on C_4 (V)
C_4 -- output capacitance (F)

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VC_4 -- peak overshoot voltage across C_4 in volts

I_{trans} -- amplitude of inductor current to be reversed in Amps

L_2 -- value of inductor in Henry

t_r -- the resonant current reversal period in seconds.

V_1 - the fundamental frequency rms value of the output voltage

V_h -- the rms magnitude at harmonic of order h.

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